

Review of Floating Point Architecture In Digital Signal Processing Applications

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Abstract: The latest development in digital signal processing (DSP) has resulted in high-speed, low-power, and reconfigurable architectures for the present communication, biomedical, and industrial applications. Developments in FIR filters, wavelet processing, approximate computing, and optimized arithmetic groups have demonstrated a high degree of improvement in area, delay, and energy consumption. Rudimentary techniques in spiking neural networks, edge-based fault diagnosis, neuromorphic computing, and photonic signal processing have emerged and make real-time intelligence and scalability even better. Advanced communication technologies like optical fiber systems, THz communication, programmable metasurfaces, joint radar-communication systems, among others, are being used to accelerate the next-generation wireless and sensing capabilities. On these developments, there are problems with the complexity of hardware, power, real-time integration, and flexibility of the system. The provided review outlines the recent accomplishments, exposes the main gaps in research, and presents the views one should adopt in the future to develop efficient, intelligent, and scalable DSP systems that will be applied in smart sensing, medical, automation, and high-speed communication systems.

I. Literature survey

In a comparative VLSI implementation, Jiménez et al. (2025) introduce the fixed-point and the floating-point multiplier topologies [1]. The paper compares array-based, Booth, Wallace tree, and other optimized designs based on delay, power, silicon area, and scalability. FPGA and ASIC synthesis are both analyzed to arrive at performance trade-offs. The authors emphasize that floating-point multipliers are more precise; however, they have high area and power overheads compared to a fixed-point design. The paper gives design advice in the choice of suitable multiplier-based architectures under the requirements of DSP, AI, or embedded applications, focusing on energy-delay product optimization in the more advanced CMOS technologies.

Haque et al. (2025) present a review of various types of multiple-input floating-point adders. The article

reviews architectures that can be supported by three or more operands, which is essential to FMA units and AI accelerators [2]. It gives comparisons between carry-save, compressor-based, and tree-based accumulation methods in the IEEE-754 compliance. The review addresses the issue of normalization, rounding issues, and pipeline optimization measures. Latency, throughput, and hardware complexity are performance metrics that are critically analyzed. The authors conclude that multi-operand adders that use compressor-trees are more scalable and energy efficient, particularly on deep-learning hardware, although without compromising numerical accuracy.

Chang et al. (2026) present a 256-point FFT processor based on analog floating-point calculation and tuned after silicon. The architecture takes advantage of arithmetic in the analog domain in order to minimize switching power in the digital domain at the expense of reasonable precision [3].



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